

WHAT IS CLAIMED IS:

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1. A transistor comprising:
a source region, a drain region, a channel region between the source and drain
5 regions, and an electrically interconnected gate formed of a silicon carbide material.

2. The transistor of claim 1, wherein the gate comprises polycrystalline silicon
carbide.

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10 3. The transistor of claim 1, wherein the gate comprises microcrystalline silicon
carbide.

4. The transistor of claim 1, wherein the transistor is a p-channel device.

15 5. The transistor of claim 1, wherein the transistor is an n-channel device.

6. The transistor of claim 1, wherein the silicon carbide gate material is described
by $\text{Si}_{1-X}\text{C}_X$ and X is approximately less than or equal to 0.5

20 7. The transistor of claim 6, wherein X is approximately equal to 0.5.

8. The transistor of claim 1, wherein the gate is separated from the channel by an
insulating layer.

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25 9. The transistor of claim 8, wherein the insulating layer is approximately between
50 angstroms and 100 angstroms thick.

10. The transistor of claim 8, wherein the insulating layer is approximately 100
angstroms thick.

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11. An integrated circuit device comprising:

a substrate;

a p-channel transistor formed in a first portion of the substrate, the p-channel transistor including a source region, a drain region, a channel region between the source and drain regions, and an electrically interconnected silicon carbide gate adjacent to the channel and separated therefrom by an insulating layer; and

an n-channel transistor formed in a second portion of the substrate, the n-channel transistor including a source region, a drain region, a channel region between the source and drain regions, and an electrically interconnected silicon carbide gate adjacent to the channel and separated therefrom by an insulating layer.

12. The integrated circuit device of claim 11, wherein the p-channel and n-channel silicon carbide gates comprise polycrystalline silicon carbide.

13. The integrated circuit device of claim 11, wherein the p-channel and n-channel silicon carbide gates comprise microcrystalline silicon carbide.

14. The integrated circuit device of claim 11, wherein the insulating layers, which separate the silicon carbide gates in each of the n-channel and p-channel transistors from their respective channel regions, are comprised of silicon oxide.

15. A semiconductor memory device comprising:

a memory array including a plurality of transistors, at least one of the transistors including an electrically interconnected gate formed of a silicon carbide material;

addressing circuitry for addressing the memory array; and

control circuitry for controlling read, write, and erase operations of the memory device.

16. A method of fabricating a transistor, the method comprising the steps of:

